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09/994,017	11/27/2001	Rene Toutant	86177-23	1111

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EXAMINER
SOL, ANTHONY M

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,017	TOUTANT ET AL.	
	Examiner	Art Unit	
	Anthony Sol	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

- Fig. 4A does not show reference number 400 mentioned in page 21, line 1.
- Fig. 5A does not show reference number 500 mentioned in page 24, line 17.
- Fig. 6 does not show reference number 600 mentioned in page 29, line 29.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6-8,10-13, 15-17 and 31-35 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,826,195 B1 ("Nikolich").

Regarding claim 1,

Nikolich shows in Fig. 8 a plurality of chassis 352, 354, 356, 358, 360, and 362. The cluster shown in Fig. 8 collectively function as a single router (Col. 8, lines 1-2). Nikolich further shows in Fig. 4 a plurality of application modules (processing modules) – CMTS, Ethernet, and SONET (Col. 3, lines 50-54). The application cards are also called data processing application module (Col. 6, lines 32-33). Nikolich also shows in Fig. 4, interchassis link port application card and chassis controller/cluster manager. The combination of interchassis link port application card and chassis controller/cluster manager is equivalent to the programmable interconnection module of the applicant.

Nikolich shows in Fig. 11 the application modules are connected to chassis controllers 428, 430 over a chassis management bus 432 (data connection between each processing module on each chassis and the interconnection module on the same chassis) (Col. 4, line 67- col. 5, line1). Nikolich further shows in Fig. 4 an inter-chassis

link port 235 through which the chassis may be linked to another chassis (data connection between the interconnection module on each chassis and the interconnection module on at least one other chassis) (Col. 3, lines 54-55).

3. Regarding claim 2,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 11 that application modules 422 (processing modules) are connected to chassis controllers 428, 430 (interconnection module) over a chassis management bus 432, which is inherently an electrical connection. Nikolich further shows in Fig. 7 that the chassis 330 and chassis 332 are linked by a full duplex link 340 that may be a Packet-over-SONET (PoS) type connection (data connections between interconnection modules on different chassis are optical) (Col. 4, lines 33-37).

4. Regarding claim 3,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 4 an interchassis link port application card. In rejection to claim 1, the combination of interchassis link port card and the chassis controller/cluster manager was established as being equivalent to the interconnection module of the applicant. The interchassis link port application card (designated as application 12 in Fig. 11) has plurality of electrical input and output ports 426. Nikolich discloses a Mesh

Communication Chip (MCC) that serves as a programmable switching fabric (Col 4. lines 57-65). Nikolich further discloses that the cluster manager keeps a centralized resource map (connection map) of all the resources, including the location of DSOs available, in the clustered system (Col. 8, lines 52-54).

5. Regarding claim 6,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 11 that each application module 422 (processing module) contains eleven serial links 426 (input and output ports) that run to the backplane (inherently electrical connection) for connecting the application module to every other application module in the chassis. The application module 422 is further connected to chassis controller 428, 430 over a chassis management bus 432 (input and output ports) (Col. 4, lines 63 – col. 5, line 1). The application cards are also called data processing application module (Col. 6, lines 31-33). The backplane is fully meshed meaning that every application module has a direct point-to-point link to every other application module in the chassis through the serial links (processing fabric disposed therebetween) (Col. 5, lines 7-9).

6. Regarding claims 7 and 8,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 11 that each application module 422 (processing module) is connected to chassis controller 428, 430 (interconnection module) over a chassis management bus 432 (inherently through electrical input and output ports) (Col. 4, lines 63 – col. 5, line 1).

7. Regarding claims 10 and 11,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 4 a plurality of application cards (Claim 10 – network interface module; Claim 11- line cards). Fig. 11 further shows various application cards 422 interfacing with an external network through the I/O port, each application card being connected to one or more electrical input and output ports of other application cards (processing modules) through links 426 and the backplane 420.

8. Regarding claim 12,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 11 that application modules 422 (processing modules) are connected to chassis controllers 428, 430 (interconnection module) over a chassis management bus 432, which is inherently an electrical connection. Nikolich further shows in Fig. 7 that the chassis 330 and chassis 332 are linked by a full duplex link 340

that may be a Packet-over-SONET (PoS) type connection (data connections between interconnection modules on different chassis) (Col. 4, lines 33-37). SONET's fiber optic lines can be OC-48 lines which is 10 gigabits per second (high-bandwidth connections) (Col. 4, lines 28-32). Relatively speaking the electrical connection between the application module and chassis controllers are inherently lower-bandwidth connections.

9. Regarding claim 13,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 11 that packets are switched inside the chassis over the MCC links 426 of the application card 422 (processing module) (Col.5, lines29-30). Fig. 11 shows the electrical input and output ports.

10. Regarding claim 15,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich discloses that each MCC 424 of Fig. 11 has one link for connecting the module with itself, i.e., a loopback.

11. Regarding claim 16,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich discloses that the cluster manager (controller) keeps a centralized resource map (connection map) of all the resources (including switch fabric), including the location of DSOs available, in the clustered system (Col. 8, lines 52-54).

12. Regarding claim 17,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 18 a craft interface. The craft interface is a network management interface using 10/100 based Ethernet, which means that it can be remote to the router (Col.7, lines 66-67).

13. Regarding claim 31,

Nikolich shows in Fig. 8 a plurality of chassis 352, 354, 356, 358, 360, and 362 (providing at least one additional chassis). The cluster shown in Fig. 8 collectively function as a single router (Col. 8, lines 1-2). Nikolich further shows in Fig. 4 a plurality of application modules (processing modules) – CMTS, Ethernet, and SONET (Col. 3, lines 50-54). The application cards are also called data processing application module (Col. 6, lines 32-33). Nikolich also shows in Fig. 4, interchassis link port application card and chassis controller/cluster manager. The combination of interchassis link port application card and chassis controller/cluster manager is equivalent to the programmable interconnection module of the applicant.

Nikolich shows in Fig. 11 the application modules are connected to chassis controllers 428, 430 over a chassis management bus 432 (data connection exists between each processing module on each additional chassis and the interconnection module on the same additional chassis) (Col. 4, line 67- col. 5, line1). Nikolich further shows in Fig. 4 an inter-chassis link port 235 through which the chassis may be linked to another chassis (data connection between the interconnection module on each additional chassis and the interconnection module on at least one original chassis) (Col. 3; lines 54-55).

Nikolich shows in Fig. 11 chassis 200 which has fourteen slots. Twelve of those fourteen slots hold application modules 205, of which may be an interchassis link port 235 through which the chassis can be linked to another chassis (Col. 3, lines 41-43 and 53-55). To link the chassis to two other chassis would require two interchassis link port card (data connection between the interconnection module one each additional chassis and the interconnection module on at least one other additional chassis).

Nikolich discloses that the chassis controller and cluster manager control the operation and configure each of the modules and can be readily modified and upgraded (Col. 3, lines 34-40) (re-programming the interconnection module on each of the original chassis).

14. Regarding claims 32 and 33,

Nikolich discloses a method that covers all the limitations of the parent claim.

Nikolich discloses that the chassis controller and cluster manager control the operation and configure each of the modules and can be readily modified and upgraded (Col. 3, lines 34-40). The word "readily" is interpreted to mean that modules can be taken off-line while modifying or programming (Claim 31 – programming the interconnection module of each additional chassis prior to the step of providing the at least one additional chassis; claim 32 - programming the interconnection module of each additional chassis after the step of providing the at least one additional chassis).

15. Regarding claims 34 and 35,

Nikolich discloses a method that covers all the limitations of the parent claim.

Nikolich shows in Fig. 7 that primary chassis 330 and secondary 332 chassises are linked by a full-duplex link 340 that may be a Fast Ethernet (Claim 34 – electrical connection) or a Packet-over SONET type connection (Claim 35 – optical connection) (Col. 4, lines 34-37).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view U.S. Patent No. 6,870,813 B1 ("Raza").

Regarding claims 4 and 5,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich does not disclose that the interconnection module on each chassis includes a signal conditioning module connected to the switch fabric.

Raza discloses that optical network systems consist of equipment, which includes various regeneration and amplification devices (Claim 4 - signal conditioning module; Claim 5 – signal conditioning functionality) (Col 6, lines 51-55).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the interconnection module of Nikolich to include/provide a regeneration and amplification device/functionality of Raza to obtain a quality signal that can be effectively switched. One skilled in the art would have been motivated to combine Nikolich with Raza (collectively "Nikolich-Raza") to generate the claimed invention with a reasonable expectation of success.

18. Claims 9, 21-23, 26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of U.S. Patent No. 6,898,205 B1 ("Chaskar").

Regarding claim 9,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 7 of Nikolich that the chassis 330 and chassis 332 are linked by a full duplex link 340 that may be a Packet-over-SONET (PoS) type connection (inherently optical input and output ports exist since SONET uses fiber optic links) (Col. 4, lines 33-37).

Nikolich does not disclose a plurality of optical-to-electrical and electrical-to-optical conversion units, each respective conversion unit being connected between a respective one of the optical input ports/output ports and a respective subset of the electrical input ports/output ports of the interconnection module.

Chaskar shows in Fig. 1 an optical interface at an optical switching node. Chaskar discloses that a control packet 170 is converted from an optical signal into an electrical signal by an optical-electrical (OE) converter 110 (Col. 3, lines 29-31). The control packet is converted from electrical domain into an optical domain in an electrical-optical (EO) converter 140 (Col. 3, lines 45-47).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the interconnection module of Nikolich to include OE and EO converters being respectively connected between a respective one of the optical input ports/output ports and a respective one of the electrical input ports/output ports as disclosed by Chaskar so that signals can be in proper format to be further routed. One skilled in the art would have been motivated to combine Nikolich

with Chaskar (collectively "Nikolich-Chaskar") to generate the claimed invention with a reasonable expectation of success.

19. Regarding claim 21,

Nikolich shows in Fig. 4 a plurality of application modules (processing modules) – CMTS, Ethernet, and SONET (Col. 3, lines 50-54).

Nikolich further shows in Fig. 11 that each application module 422 (processing module) contains eleven serial links 426 (input and output ports) that run to the backplane (inherently electrical connection) for connecting the application module to every other application module in the chassis. The application module 422 is further connected to chassis controller 428, 430 over a chassis management bus 432 (input and output ports) (Col. 4, lines 63 – col. 5, line 1). The application cards are also called data processing application module (Col. 6, lines 31-33). The backplane is fully meshed meaning that every application module has a direct point-to-point link to every other application module in the chassis through the serial links (processing fabric disposed therebetween) (Col. 5, lines 7-9).

Nikolich also shows in Fig. 4, interchassis link port application card and chassis controller/cluster manager. The combination of interchassis link port application card and chassis controller/cluster manager is equivalent to the programmable interconnection module of the applicant.

Nikolich also shows that the interchassis link port application card (designated as application 12 in Fig. 11) has plurality of electrical input and output ports 426. Nikolich

discloses a Mesh Communication Chip (MCC) that serves as a programmable switching fabric (Col 4. lines 57-65). Nikolich further discloses that the cluster manager keeps a centralized resource map (connection map) of all the resources, including the location of DSOs available, in the clustered system (Col. 8, lines 52-54).

Nikolich also shows in Fig. 11 that each application module 422 (processing module) is connected to chassis controller 428, 430 (interconnection module) over a chassis management bus 432 (inherently through electrical input and output ports) (Col. 4, lines 63 – col. 5, line 1).

Nikolich shows in Fig. 7 of Nikolich that the chassis 330 and chassis 332 are linked by a full duplex link 340 that may be a Packet-over-SONET (PoS) type connection (inherently optical input and output ports exist since SONET uses fiber optic links) (Col. 4, lines 33-37).

Nikolich does not disclose a plurality of optical-to-electrical and electrical-to-optical conversion units, each respective conversion unit being connected between a respective one of the optical input ports/output ports and a respective subset of the electrical input ports/output ports of the interconnection module.

Chaskar shows in Fig. 1 an optical interface at an optical switching node. Chaskar discloses that a control packet 170 is converted from an optical signal into an electrical signal by an optical-electrical (OE) converter 110 (Col. 3, lines 29-31). The control packet is converted from electrical domain into an optical domain in an electrical-optical (EO) converter 140 (Col. 3, lines 45-47).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the interconnection module of Nikolich to include OE and EO converters being respectively connected between a respective one of the optical input ports/output ports and a respective one of the electrical input ports/output ports as disclosed by Chaskar so that signals can be in proper format to be further routed. One skilled in the art would have been motivated to combine Nikolich with Chaskar (collectively "Nikolich-Chaskar") to generate the claimed invention with a reasonable expectation of success.

20. Regarding claims 22 and 23,

Nikolich-Chaskar discloses a system that covers all the limitations of the parent claim.

Nikolich-Chaskar shows in Fig. 4 of Nikolich a plurality of application cards (Claim 22 – network interface module; Claim 23- line cards). Fig. 11 further shows various application cards 422 interfacing with an external network through the I/O port, each application card being connected to one or more electrical input and output ports of other application cards (processing modules) through links 426 and the backplane 420.

21. Regarding claim 26,

Nikolich-Chaskar discloses a system that covers all the limitations of the parent claim.

Nikolich-Chaskar shows in Fig. 11 of Nikolich that packets are switched inside the chassis over the MCC links 426 of the application card 422 (processing module) (Nikolich, col.5, lines29-30). Fig. 11 shows the electrical input and output ports.

22. Regarding claim 28,

Nikolich-Chaskar discloses a system that covers all the limitations of the parent claim.

Nikolich-Chaskar discloses that each MCC 424 of Fig. 11 of Nikolich has one link for connecting the module with itself, i.e., a loopback.

23. Regarding claim 29,

Nikolich-Chaskar discloses a system that covers all the limitations of the parent claim.

Nikolich-Chaskar discloses that the cluster manager (controller) keeps a centralized resource map (connection map) of all the resources (including switch fabric), including the location of DSOs available, in the clustered system (Nikolich, col. 8, lines 52-54).

24. Regarding claim 30,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich-Chaskar shows in Fig. 18 of Nikolich a craft interface. The craft

interface is a network management interface using 10/100 based Ethernet, which means that it can be remote to the router (Nikolich, col.7, lines 66-67).

25. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of Chaskar, and further in view of Pub. No. U.S. 2002/0150056 A1 ("Abadi").

Nikolich-Chaskar discloses a system that covers all the limitations of the parent claim.

Nikolich-Chaskar does not disclose that the programmable switch fabric implements a non-blocking switch

Abadi discloses that crossbar 12 of Fig. 2 is a non-blocking switch.

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the switch fabric of Nikolich-Chaskar to have a non-blocking capability as disclosed by Abadi so that the packets are switched efficiently. One skilled in the art would have been motivated to combine Nikolich-Chaskar with Abadi (collectively "Nikolich-Chaskar-Abadi") to generate the claimed invention with a reasonable expectation of success.

26. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of Chaskar, further in view U.S. Patent No. 6,870,813 B1 ("Raza").

Regarding claims 24 and 25,

Nikolich-Chaskar discloses a system that covers all the limitations of the parent claim.

Nikolich-Chaskar does not disclose that the interconnection module on each chassis includes a signal conditioning module connected to the switch fabric.

Raza discloses that optical network systems consist of equipment, which includes various regeneration and amplification devices (Claim 24 - signal conditioning module; Claim 25 – signal conditioning functionality) (Col 6, lines 51-55).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the interconnection module of Nikolich-Chaskar to include/provide a regeneration and amplification device/functionality of Raza to obtain a quality signal that can be effectively switched. One skilled in the art would have been motivated to combine Nikolich-Chaskar with Raza (collectively "Nikolich-Chaskar-Raza") to generate the claimed invention with a reasonable expectation of success.

27. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of Abadi.

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich does not disclose that the programmable switch fabric implements a non-blocking switch

Abadi discloses that crossbar 12 of Fig. 2 is a non-blocking switch.

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the switch fabric of Nikolich to have a non-blocking capability as disclosed by Abadi so that the packets are switched efficiently. One skilled in the art would have been motivated to combine Nikolich with Abadi (collectively "Nikolich-Abadi") to generate the claimed invention with a reasonable expectation of success.

28. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikolich in view of U.S. Patent 6,058,116 ("Hiscock").

Regarding claim 18,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 4 that each chassis includes a interchassis link port 235 (one port reserved for intra-cluster connection).

Nikolich does not disclose that the chassis are arranged in two or more clusters. Nor does he disclose that the chassis has at least one port reserved for inter-cluster connection.

Hiscock shows in Fig. 7 the concepts of interconnect trunk cluster 110 (two or more clusters). One logical port of each trunk switch 120 is connected to trunk port 137 (one port reserved for inter-cluster connection) (Col. 8, lines 46-49).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the chassis of Nikolich to include having an arrangement of two or more clusters and having one port of a trunk be connected to another port of a trunk in a different cluster as taught by Hiscock so that the clusters can act as a single router. One skilled in the art would have been motivated to combine Nikolich with Hiscock (collectively "Nikolich-Hiscock") to generate the claimed invention with a reasonable expectation of success.

29. Regarding claim 19,

Nikolich discloses a system that covers all the limitations of the parent claim.

Nikolich shows in Fig. 4 a chassis with an interchassis link port card (chassis interconnection module) that connects to all the chassis in cluster (connections between chassis of a particular one of the clusters are established through the chassis interconnection module).

Nikolich does not expressly disclose that the chassis are arranged in two or more clusters. Nor does disclose that the connection between each pair of clusters are established through the chassis interconnection modules of the clusters of said pair.

Hiscock shows in Fig. 8 two trunk clusters 110 and 210 (two or more clusters). Fig. 8 further shows that the two clusters are connected by links 125 connecting GEN 2 devices (connection between clusters are through chassis interconnection modules) (Col. 9, lines 6-7).

It would have been prima facie obvious to one of ordinary skill in the art at the time of the invention was made to modify the chassis of Nikolich to include having an arrangement of two or more clusters and where the clusters are interconnected by a trunk device such as the GEN 2 as taught by Hiscock so that the clusters can act as a single router. One skilled in the art would have been motivated to combine Nikolich with Hiscock (collectively "Nikolich-Hiscock") to generate the claimed invention with a reasonable expectation of success.

30. Regarding claim 20,

Nikolich-Hiscock discloses a system that covers all the limitations of the parent claim.

Nikolich-Hiscock further discloses that the cluster manager keeps a centralized resource map (programmable connections) of all the resources (between different chassis in cluster and between chassis in said cluster and chassis interconnection module of other clusters), including the location of DSOs available, in the clustered system (Nikolich, col. 8, lines 52-54).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Sol whose telephone number is (571) 272-5949. The examiner can normally be reached on M-F 7:30am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AMS

AMS

7/21/2005

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600